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September 2019

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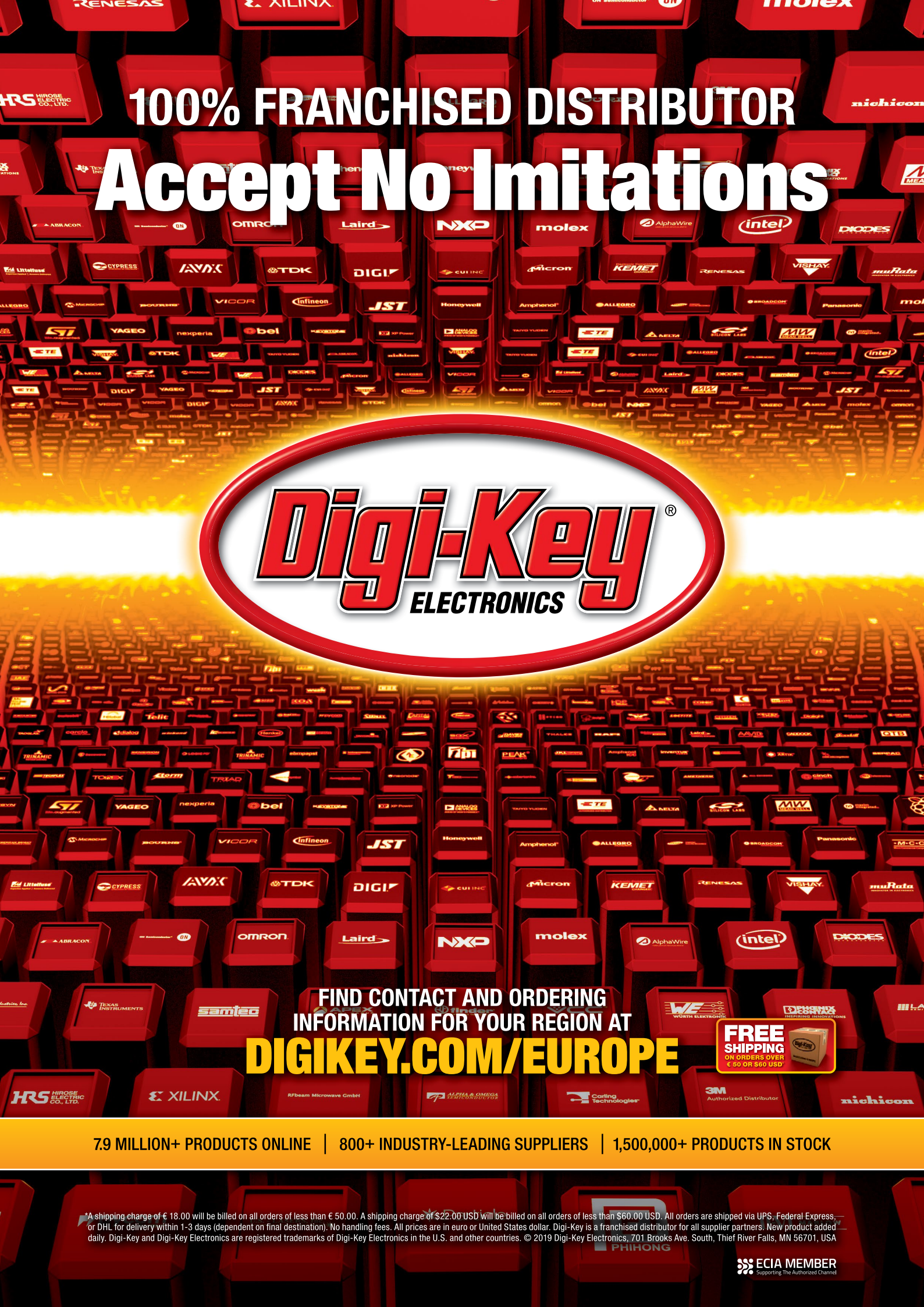
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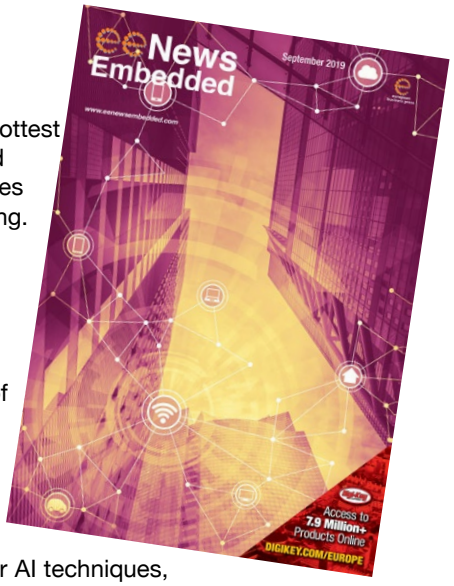

Dear readers,

Welcome to the September issue of eenews Embedded. In this issue, we look at three of the hottest topics in the industry. Our first subject is probably the most important technology in embedded systems today. The IoT offers a huge potential to improve our health, our homes, our workplaces and our environment by continuously monitoring the condition of almost anything and everything.

The data gathered by sensors is processed and stored to provide us with short- and long-term trends that are actionable. It can be processed both locally on the edge, or remotely in the cloud. In either case, a secure, reliable connection is required. In most cases, this connectivity will be wireless - our second featured subject this month. There are many different wireless standards available to developers, and inside we look at which protocol is best for each type of application.

Our third featured topic this month is also highly relevant to the efficient implementation of the IoT. FPGAs provide the high performance and throughput that is required to process the data flowing in from a multitude of sensors in a timely enough fashion that allows action to be taken in time. They also offer the flexibility to be reconfigured to keep up with new standards or AI techniques, making them ideal for use in the cloud and at the edge.

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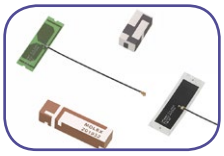

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Design your own far-field voice interface

This month, XMOS is giving away three VocalFusion Dev Kits for Amazon AVS (XK-VF3510-L71-AVS) for eeNews Europe's readers to evaluate and prototype far-field voice interfaces using the XVF3510 voice processor with the Amazon Alexa Voice Service. Worth $399, the VocalFusion development kit is a far-field 2-mic solution optimised for smart TVs and set-top boxes. It is built around the XMOS XVF3510 voice processor, running the company's next generation acoustic algorithms to support far-field voice capture with close range precision. Only costing $0.991, the XVF3510 enables manufacturers to embed a voice interface into mass-market smart TVs and set-top boxes economically. Developed in the UK and purpose-built for modern living spaces, XMOS' next generation acoustic algorithms can identify and isolate a voice command from every other sound in the room (including any media streaming through the device itself). They include a stereo acoustic echo canceller, an interference canceller to cancel out unwanted background noise, and an adaptive delay estimator that dynamically adjusts audio reference signal latency, ensuring the acoustic echo cancellation algorithms deliver a smooth, real-time experience.

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Xilinx FPGAs Accelerate Artificial Intelligence Inferencing at SK Telecom

Daniel Eaton, Xilinx

The massive parallelism and reconfigurability of Xilinx Kintex UltraScale FPGAs enabled SK Telecom to enhance both the speech-recognition accuracy and response time of its NUGU voice-activated assistant, while also gaining the flexibility to evolve its Automatic Speech Recognition platform with the advancing state of the art in Artificial Intelligence.

Artificial Intelligence (AI) is quickly penetrating markets for online consumer services, and major players are moving quickly to upgrade their data centres accordingly. Low-latency inference is a key requirement, to ensure applications such as voice recognition deliver a seamless user experience. In addition, while cost, power consumption, and time to market are key concerns, flexibility is essential to keep pace with the rapid technological advancements in AI without incurring high ownership costs.

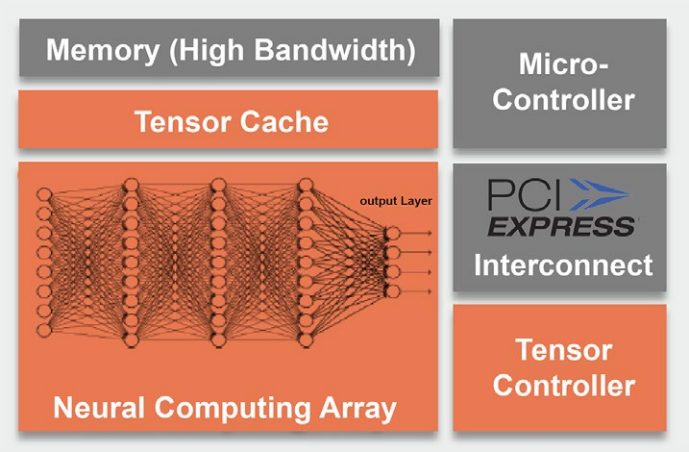

Figure 1. SK Telecom's NPU in Xilinx Kintex UltraScale FPGAs powers the AIX accelerator for NUGU's ASR servers.

Large cloud and telecom operators agree that traditional hardware platforms for neural networks are unable to meet the demands of large-scale commercial deployment. One such company, SK Telecom, has successfully deployed AI accelerators at its data centers in South Korea, and has achieved extremely high performance with low latency by working with Xilinx to maximize the benefits of FPGA parallelism and power efficiency. At the same time, FPGAs allow flexibility to upgrade the accelerators quickly with even more advanced neural networks as AI technology continues to move forward at a rapid pace.

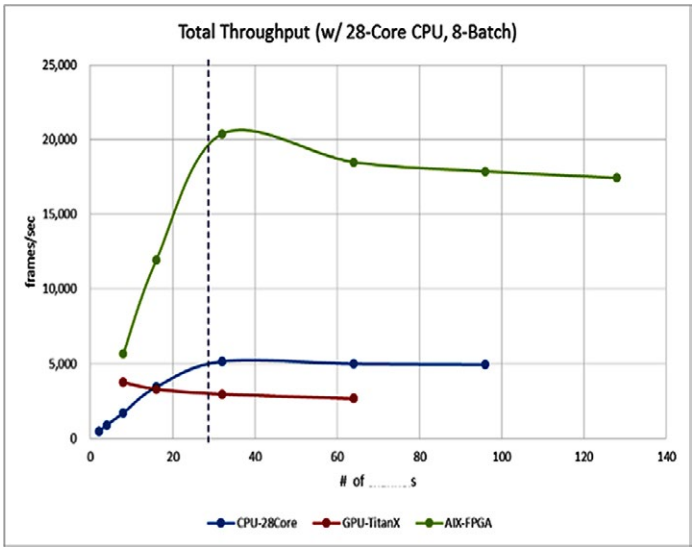

Figure 2. SK Telecom diagram - Throughput vs number of channels comparing GPU and FPGA accelerators vs CPU-only servers.

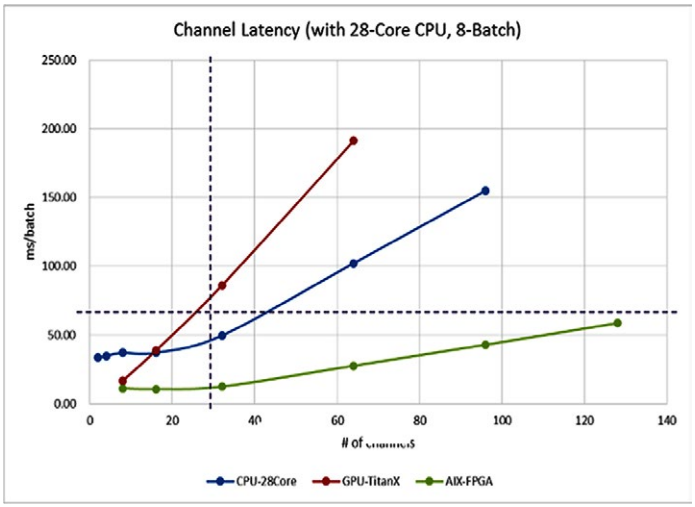

Figure 3. SK Telecom diagram - Latency vs number of channels.

SK Telecom is Korea's largest telecommunications company. With more than 29 million mobile subscribers, around 50 percent of the total market, the company is currently developing a portfolio of AI-based services including NUGU; the first digital home assistant to work in Korean language. NUGU already provides music and smart-home support, information on demand, smartphone-location tracking, diary assistance, and more features are planned for the future including open APIs to let third-party developers enter the ecosystem.

NUGU incorporates SK Telecom's expertise in artificial intelligence, speech recognition, and natural language processing. Capable of understanding voice tones, accents, and dialects, it achieves a very high voice-recognition rate. With SK Telecom's natural language processing engine at its heart, it can interpret the user's wishes accurately and interact by voice.

"In addition to ultra-reliable recognition, we knew that delivering the best possible user experience would depend on instant response to any query at any time," says Lee Kang-Won, senior vice president and head of Software Labs at SK Telecom. "To achieve this, we set out to build AIX, our AI Inference Accelerator. It contains multiple custom NPUs that we optimised for low-latency voice recognition and implemented on Xilinx FPGAs for flexibility and a fast time to market."

Inference describes the function of the neural network after having been trained and deployed. Deploying trained models for inference has become one of the most important challenges to the commercialization of AI: whereas the tools for training neural networks are more affordable and easier to use than ever, industry experts say the cost of deploying models for inference is now the largest contributor to infrastructure cost over time.

As far as performance is concerned, extremely low latency is critical for voice-based services that interact directly with human end-users, as SK Telecom's Lee Kang-Won has observed. Consumers expect a natural and seamless experience, which calls for near real-time inference. Techniques for achieving this are still developing, as more and more operators set out on the AI-deployment journey. In contrast, much is already known about training neural networks. For this, large GPU arrays have become the platform of choice to handle the many exabits of data and teraflops of compute, but training is done offline and can be completed over days or weeks. When it comes to deployment, the application must deliver the expected performance within stringent latency and power consumption requirements.

Xilinx has shown that FPGA accelerators deliver the real-time inferencing response needed for speech recognition and natural language interaction at much lower power consumption than is possible using GPUs. On the other hand, although an ASIC-based inferencing engine could combine low latency with low power consumption, FPGA accelerators give the added advantage of reconfigurability to adopt the latest machine-learning technologies quickly as they continue to evolve.

The team at SK Telecom based its AIX on Xilinx KCU1500 datacentre accelerator cards containing Kintex UltraScale XCKU115 FPGAs. The AIX contains a large array of neural cores implemented in the DSP slices of Kintex FPGAs to run the automatic speech-recognition (ASR) application at the heart of NUGU.

The neural array and associated functions including weight feeder, tensor cache, and tensor controller (figure 1) create a high-performance Neural Processing Unit (NPU) that effectively contains tens of thousands of accelerators for inference: ultimately providing much greater parallelism than is possible with a GPU. By applying static and dynamic computation optimization, with pruning, quantization, and dynamic precision, SK Telecom's engineers have ensured that over 95% of the FPGAs' DSP cores are active on every cycle.

SK Telecom populated its existing CPU-only ASR servers with the KCU1500 PCIe Gen 3 x16 accelerator cards. The teams' own figures point to a 500% performance improvement when running multiple concurrent voice channels compared to experience with GPU-based accelerators (figures 2 and 3). Moreover, consuming less than one-third of the power translates into a 16-fold improvement in performance per Watt.

In addition, the reprogrammable nature of the Kintex UltraScale FPGAs gives SK Telecom the flexibility to adopt new and improved neural network architectures in the future, while at the same time delivering the solution within a tight timeframe.

Conclusion

Following successful introduction of the AIX cards, SK Telecom's project represents the first commercial adoption of FPGA accelerators in the AI domain for large-scale data centers in South Korea. The adaptive nature of the Kintex UltraScale FPGAs allow the team to continue developing new and improved custom hardware accelerators, keeping pace with the state of the art in AI and deep learning.

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Easing FPGA Integration in Data Centres

Intel

The significant execution and power performance of FPGAs is driving their growing use in multiple applications, such as signal processing, cryptography and deep learning inference. FPGAs use massive parallelism and deep pipelining techniques to perform highly compute-intensive loops in hardware, offloading these "kernels" from software and enabling substantial improvements in execution speed.

The growth of cloud computing is seeing more and more of such compute-intensive applications, including artificial intelligence (AI), big-data analysis and traditional supercomputing applications being undertaken within cloud and enterprise data centres. FPGA acceleration offers some obvious advantages in this environment, which some public cloud providers have already recognised, but traditional data centre development tools, processes and culture, inhibit widespread adoption of FPGAs.

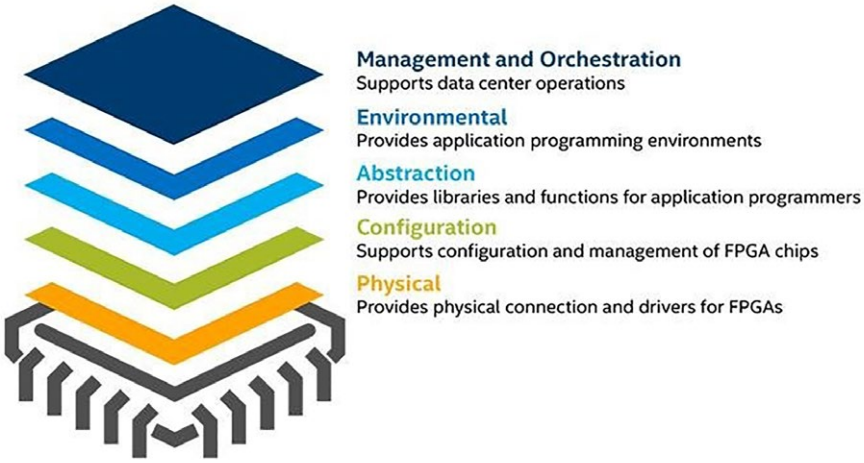

Figure 1. An adaptation stack represents the tasks and tools necessary to make FPGA acceleration accessible to users.

This article looks at the two areas where FPGA and traditional data-centre development are most mismatched – programming and management and orchestration, (MANO) – and then proposes an approach to bridging this gap.

Inhibitors to FPGA integration

The term "programming" may be used for both FPGAs and traditional CPUs, but the tasks involved, and skills required are very different for each type of device. With the traditional CPU, developers write code in high-level languages, at a level of abstraction from the "black-box" CPU and the programming development environment translates the high-level code into machine-level instructions. This type of programming requires no knowledge of the underlying hardware and with certain exceptions, the programmer doesn't have to worry about timing and sequencing of instructions.

FPGA programming also starts with human-readable languages, such as C++, but programming involves descriptions of hardware structures and logic blocks, rather than sequences of instructions. FPGA programming requires the developer to get involved in specifications of timing constraints and sequences and the process is much closer to hardware configuration than CPU programming.

Whilst the development culture is therefore very different for traditional data centre technologies and FPGAs, established data centre administration techniques also struggle to accommodate FPGAs.

Modern data centres are highly automated environments built on a multitude of identical racks containing similar servers sharing network connections and storage nodes. Increasingly, virtualisation is being used to enable rapid switching of data centre resources across servers and MANO tools enable resource tracking, scheduling and billing. FPGAs do not fit easily into this environment; unlike the traditional server they are not identical, their power coming from their variety. Consequently, although they can be reconfigured when required, this cannot be done within the nano-second windows required by data-centre MANO tools.

The challenge therefore is to find ways of making the power of FPGAs available to the application developer and end users by bridging this mis-match between tools, processes and culture.

The Stack

If the use of FPGAs is to be made transparent at the high level to data centre developers, then it will not suffice to simply insert a card with an FPGA into a server slot; more work is required to achieve the level of abstraction required in this environment.

The OSI model, (Open Systems Interconnection model), adopted in the telecommunications world serves as a useful tool to address this bridging challenge and for this purpose a five-layer model or "stack" is defined, as shown in figure 1.

For this specific purpose, 5 layers are required – physical, configuration, abstraction, environmental and MANO - as described in the following sections.

Physical Layer

To gain access to the full capabilities of the FPGA it should be placed on its own card and plugged into the data centre server rack, following the approach adopted by Intel with its Intel Stratix 10 Programmable Accelerator Card. This enables the FPGA's serial ports to have access to the backplane network, facilitating communication with a particular CPU via PCI Express. In this configuration, the FPGA is able to work as a slave accelerator to the CPU or, alternatively, can stream data directly from the network.

Further work is required at this level however to make the FPGA a useful accelerator; FPGA, CPU and server board designers need to cooperate at this level to create a hardware "gasket", or signal bridge, containing user-designed functions to enable the FPGA to talk to its host CPU, maintain security, transfer data and manage execution.

Device drivers integrated with the operating system kernel then make these control and supervision functions available to higher layers of the stack.

Configuration

A wide range of programming and configuration support exists to help developers working with FPGAs. At one end of the spectrum are tools which map a C++ program almost directly to an FPGA configuration, aimed at developers with no hardware skills to tools which enable configuration directly in Hardware Description Language, (HDL).

Recent developments include a higher-level tool which supports parallelism, pipelining and streaming and works alongside the industry-standard OpenCL language. This enables a developer to separate his algorithm into a control block, written in C and which runs on a CPU and one or more kernels for acceleration. The toolset manages the execution of the control block on the CPU and the kernels on the specified FPGA resources, removing the need for FPGA expertise and reducing deployment time.

Tools such as this, including Intel Parallel Studio, greatly simplify the process of identifying opportunities for acceleration and implementing them in kernels.

Abstraction

Many application developers will have little interest in acquiring the level of skill required to interact with FPGA tools and will look for a higher level of abstraction. From their point of view, the ideal would be to have access to a set of libraries, which would take care of accelerator initialisation and FPGA acceleration of specific functions.

Indeed, some of this capability is now in place, with a number of libraries which cut across applications already widely used. These libraries are set to develop as FPGA deployment in the cloud increases and we can expect the emergence of specialised libraries, targeting specific fields, such as structural or fluid analyses, physical chemistry or genetics.

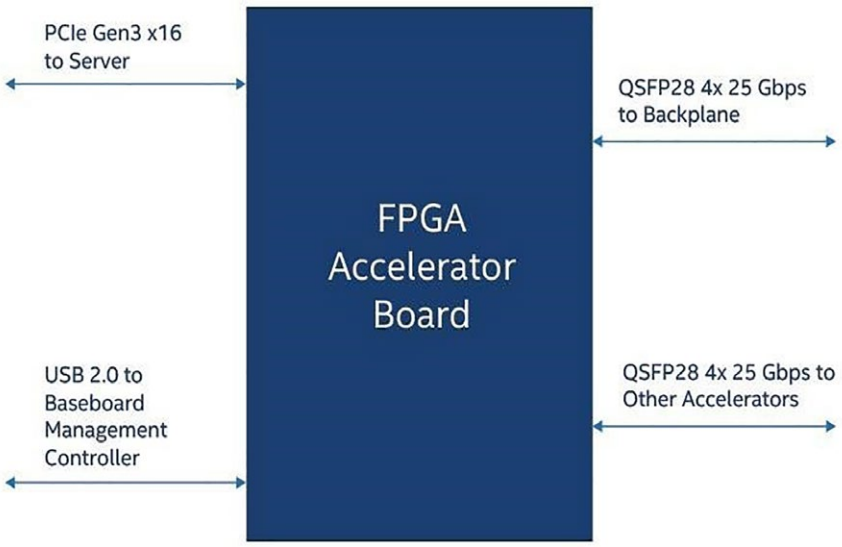

Figure 2. Possible FPGA to data-centre fabric connection routes

Further trends will see even more levels of abstraction for the user with integration of FPGA acceleration into application frameworks, for machine learning, data analytics or video coding, for example.

Beyond that, turnkey applications will emerge which will request and apply FPGA acceleration from the data centre transparently; the end user will be oblivious to the level of effort which will have gone into libraries but will experience shorter execution times and/or higher throughput.

Environmental

Whatever the specifics of the underlying FPGA implementation, DevOps personnel in the datacentre will require access to the same debug environment as for any other cloud application. However, in order to give users the ability to debug their code at source level, as they are used to, a number of issues must be addressed for FPGA-accelerated packages.

To carry out steps such as loading of configuration files, reading and writing of FPGA memory, initialisation of FPGA logic and starting and stopping execution, FPGA debug environments need access to the chip's drivers. This requires support from the FPGA gasket logic as well as driver code on the CPU and explicit inclusion of debug structures in the user's logic design.

At this level, there are tools available which provide a level of FPGA simulation useful to the application developers, allowing them to conduct high-level debugging in a software-only environment.

Mano

Within the cloud data centre many tasks run which have nothing to do with the execution of user code. Resource availability tracking, billing support and update deployment are all management tasks. Orchestration tasks assign computing, network and storage resources to tasks, whilst at the same time optimising resource utilisation and task performance. The creation of virtual machines, their binding to physical resources and their protection for each other are all functions performed by hypervisors. FPGA accelerators present specific challenges to all three of these functions.

Management automation software must discover the version of gasket code currently installed in the FPGA, the user functions that are installed and the resources currently available for further functions. Open standard interfaces such as Intel's Open Programmable Accelerator Engine are available which enable the management automation software to gain access to this information via the FPGA's drivers.

Orchestration software needs to know the status of resources already programmed into the FPGA and those which remain uncommitted. It also needs to know which of the options depicted in figure 2 are used to connect the chip to the data-centre fabric. At the same time, it must have visibility of the FPGA's internal memories and must make decisions on whether to preserve or erase the chip's configuration.

Hypervisors are also challenged by the heterogeneous characteristics of FPGAs, as they are used to the uniform fabric of the data centre.

www.intel.com

Zynq UltraScale+ module offers 38.4 GByte/s memory bandwidth

Enclustra's new Mercury+ XU9 SoC module has 20 multi-giga-bit transceivers that offer data rates of up to 15 Gbit/s each and an overall memory bandwidth of up to 38.4 GByte/s.

The Mercury+ XU9 module has been designed around a 16 nm FinFET+ Xilinx Zynq UltraScale+ MPSoC, which has 6 ARM cores, a Mali-400MP2 GPU (EV variant), up to 12 GByte DDR4 SDRAM, standard interfaces, 192 user I/Os and up to 504,000 LUT4 equivalents.

The sixth member of Enclustra's SOM family based on Xilinx' Zynq UltraScale+ MPSoC, the module has two memory banks - a 64-bit wide DDR4 SDRAM (up to 4 GByte) connected to the PL and a 72-bit DDR4 ECC SDRAM (up to 8 GByte) connected to the PS.

Measuring only 74 × 54 mm, the module offers many interfaces, including two Gigabit Ethernet and USB 3.0 ports, DisplayPort, SATA, and SGMII. It also offers a 16 GByte eMMC and 64 MByte QSPI Flash. PCIe connections are available on both the processing system and the FPGA matrix.

Enclustra also offers support for its products, including the Mercury+ PE1-300 and Mercury+ PE1-400 baseboards, which provide a complete hardware development platform with the Mercury+ XU9. The company also provides software and support materials for the XU9. Enclustra Build Environment can compile Linux for the Enclustra SoC modules with integrated ARM processors very smoothly. After using a GUI to select module and baseboard, the Enclustra Build Environment downloads the appropriate Bitstream, First Stage Boot Loader (FSBL) and the required source code. Finally, U-Boot, Linux and the root file system based on BusyBox are compiled.

Enclustra
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World's Largest FPGA has 9 million system logic cells

Xilinx has expanded its 16nm Virtex UltraScale+ family to now include the Virtex UltraScale+ VU19P - the world's largest FPGA.

The VU19P has 35 billion transistors to provide the highest logic density and I/O count on a single device. It features 9 million system logic cells, has up to 1.5 terabits per-second of DDR4 memory bandwidth and up to 4.5 terabits per-second of transceiver bandwidth, as well as over 2,000 user I/Os.

The VU19P is 1.6X larger than the 20 nm Virtex UltraScale 440 FPGA, its predecessor which used to hold the crown for the largest FPGA.

The VU19P has comprehensive support with debug, visibility tools, and IP for speedy design and validation. Hardware and software co-validation helps to bring up software and implement custom features before physical parts are available. The design flow can also be co-optimised by using the Xilinx Vivado Design Suite, reducing risk and cost.

Xilinx
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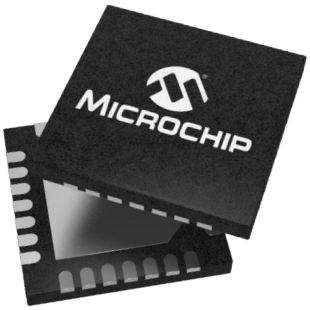

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Developing an Effective Antenna for IoT Applications

Matt McWhinney, Molex

Access to the internet is no longer restricted to devices intended for people; things that we may never interact with directly now account for billions of connections and that number is only going up. As vehicles become more connected, we will see increased demand for V2X solutions, the rollout of 5G services will allow even more connectivity, while location-based services are increasing demand for GPS and GNSS functionality. All of these applications rely on wireless communications and, in many cases, they will be hidden from sight, located deep within large machines, vehicles or even structures like bridges.

The data that these things produce is increasingly mission-critical and so developing robust devices able to maintain a connection under sometimes difficult conditions is even more important. With an increasing number of System-on-Chip (SoC) and System-in-Package (SiP) devices available with fully integrated RF interfaces, accessing wireless connectivity is now simpler than ever, however there is one aspect that still needs special consideration to achieve optimum performance; the antenna.

Link budgets are critical in delivering reliable communications and perhaps the single most important part of developing an RF interface. The antenna selection and, more crucially, the way it is designed into the system will have a major influence on the link budget. Because of this, understanding and following well established RF antenna guidelines forms an important part of the overall design process.

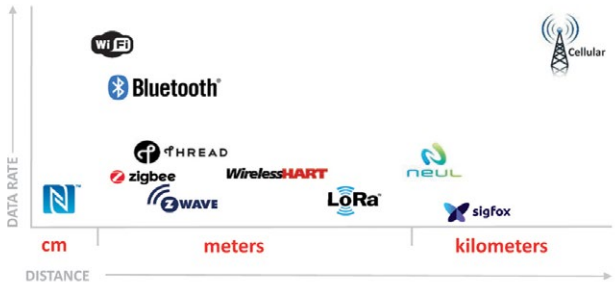

Figure 1: RF is now used in more applications, driving the development of protocols to meet the needs of specific application types

The basics of antenna theory

We now experience many forms of wireless connectivity in our digital lives, with little consideration for the antenna used, but they are clearly the single most influential component in an RF system.

In theory, any conductive wire can be an antenna, as it will be capable of radiating and receiving RF energy through the air. However, in order to do this reliably it is necessary to take this theory and apply engineering know-how. The challenge many design engineers face today is how to achieve this optimal design without the benefit of a full understanding of the nuances of RF design.

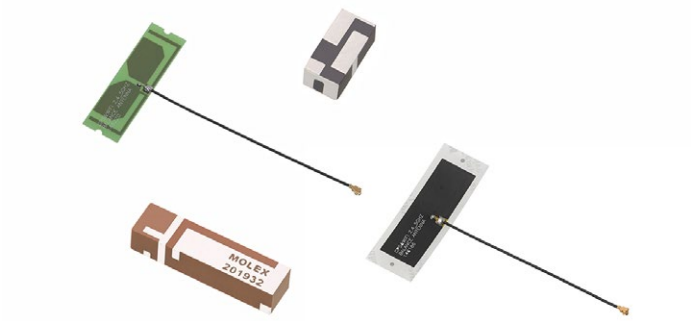

Figure 2: Antennas come in a various shapes, sizes and materials. Choosing the right one isn't always simple

The first thing to appreciate is that antennas are indiscriminate, by which we mean they do not really care what the energy (signal or protocol) contains, they are merely concerned with its presence (frequency) and levels (strength). It is the modulation scheme that carries the real data and in order for the backend to recover this it is important that the antenna is designed in sympathy with this. In fact, an antenna will behave in exactly the same way when it is both receiving and transmitting; known as the theory of reciprocity. Of course, this also means that it doesn't really matter if the device is a transmitter, a receiver or both, the antenna design will be the same.

In terms of the devices typically being deployed as part of the IoT, an antenna will be classed as either embedded, meaning it would be mounted directly on the PCB and connected using copper tracks, or cabled, which means it is connected to the PCB using a (normally coaxial) cable. Cabled antennas are often mounted inside the enclosure, but of course, antennas may also be mounted outside the main enclosure or, in some cases, on the outside of a building.

As part of the antenna design or selection it is relevant to consider several criteria, including the data rate needed, the frequencies being used and range of the wireless connection, which will impact the system power levels. Many of these criteria will be common across a range of applications and so it is not surprising to know that they are already defined in specifications for wireless protocols, such as Bluetooth, Wi-Fi, LoRa and many others targeting the IoT and various other applications, such as wireless networking and remote metering.

Range is perhaps the most basic parameter that can help when determining the most appropriate protocol for a given application. This will cover short, medium and long range, spanning less than 10cm to many kilometres, respectively. Range is also closely related to data rate and this can often be a bigger determining factor than range, although of course the two are both largely dependent on power. Some protocols support only

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Figure 3: Wireless protocols are typically differentiated by range, data rate and applications, even those that operate at the same frequency

very low data rates but over long distances and at relatively low power levels, while higher data rates are typically restricted to shorter distances but may still require more system power to function.

Operating frequency is also defined by the protocol and most engineers will be at least somewhat familiar with the license-free bands allocated for Industrial, Scientific and Medical (ISM) applications and, within these, the 2.4GHz band used by many of the most popular protocols. Despite using the same part of the spectrum, these protocols offer various ranges and data rates, which influences both their relative power requirements and the overall cost of radio devices. It is important to realise that the RF electronic circuitry defines the protocol, whereas the antenna simply receives and transmits RF signals fed to it by the electronics, irrespective of the protocol used.

This means that while the RF SoC/SiP used may differ between protocols, it is actually possible to use the same antenna design for any protocols that operate at the antenna's intended frequency, such as those operating at 2.4GHz (WiFi, Bluetooth, Zigbee, etc.). This means, of course, that one antenna can support several protocols. Having said that, there remain other relevant considerations when selecting an antenna, such as the physical space available and its location within the product. This will define the shape of the antenna, which may need to conform to a given profile in order to support the required frequency or bandwidth.

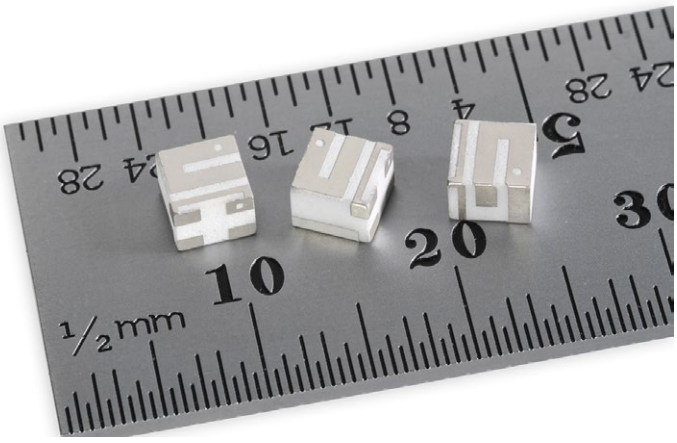


Figure 4: Antennas can be designed and manufactured to meet the most demanding space constraints

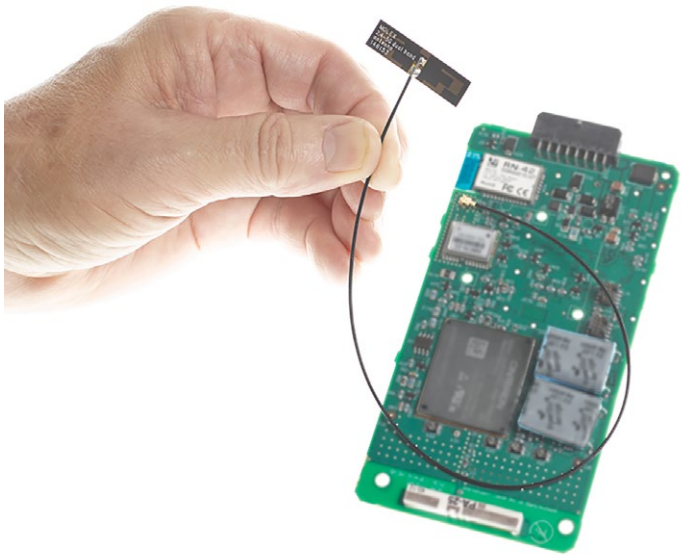


Figure 5: Design options include PCB-mounted and remotely located. Often, the application will dictate the most appropriate approach

Antenna design expertise

Molex has been designing, manufacturing and supplying standard and custom integrated antennas for two decades, for mobile and IoT applications in various volumes and for leading device manufacturers around the world.

The Molex antenna product portfolio covers all the major protocols used today, as well as proprietary solutions, with a focus on embedded (PCB mounted) and internal cabled antennas, when performance requirements may dictate their use.

Embedded antennas can be extremely small and manufactured from ceramic and plastic, as well as stamped metal, weighing just a few grams (Figure 4). Cabled antennas can be made using PCBs, both rigid (FR4) and flexible, as well as stamped metal. These capabilities make it simple to find the most appropriate antenna design, whatever the application. Even though they can be made very small and compact, embedded antennas still come with design requirements that, if followed, will help ensure that the antenna performs as the specification demands. Many factors, such as the size of the PCB, its shape and where the antenna is mounted on the PCB can all impact how the antenna performs.

To support the product portfolio, Molex has produced a library of application specifications. These are engineering documents that go beyond the standard antenna data sheet. They include not only performance information but a reference design, with advice on where and how to locate the antenna on a PCB. Perhaps most importantly, the application specification provides an estimate of the antenna's operation and how this will vary based on its location on a PCB, taking into account its proximity to other components and features such as batteries, metal shields and the cable itself for cabled antennas. These application specification documents provide essential guidelines that system designers should read to understand how to best engineer the antenna into each system.

In most cases, the information provided in the application

Figure 6: Molex offers a wide variety of antennas and the expertise to develop the right solution for any application

specification has been simplified to make it more easily accessible to engineers with varying levels of RF expertise, and of course Molex can also provide access to an expert if and when required. In many instances, it is advised that design teams placing antennas into their systems seek assistance and guidance from an RF expert. This can save time when it comes to understanding what additional measures are needed to boost antenna performance and quantitatively measuring antenna performance in a system.

To support its customers, Molex has also invested in antenna measurement technology, including field-scanning chambers to support product development, up to frequencies used in 5G transmissions. When used alongside its advanced simulation capabilities, this enables Molex to develop antennas that deliver high performance while still complying with SAR (Specific Absorption Rate) specifications. Once designed, Molex can also manufacture custom antennas, to meet the customer's production needs. Molex not only designs antennas; its RF engineers are experts and are ready to assist customers' design engineers investigate and document the performance of antennas in a system. If your application requires improved RF performance, consider turning to a Molex RF expert for assistance.

https://www.molex.com

Bluetooth 5 module delivers more range and flexibility

Laird Connectivity's new BL654 PA (Power Amplified) series of Bluetooth modules provide more power and range than ever before.
BL654 PA also has maximum design flexibility and performance. It is a full multi-protocol embedded wireless module with exceptional processing capability and extended PA/LNA support.
The module is centred around the Nordic nRF52840 solution. It has a small form factor and provides a secure, robust BLE and Cortex-M4F CPU for applications. The BL654 PA has programming options for both an intuitive AT command set and Laird Connectivity's own smartBASIC environment.
smartBASIC is an event-driven programming language to make integration easier. The language offers built-in functions that replace hundreds of lines of C code. It also acts as a bridge between software and hardware, allowing an application to work on any smartBASIC radio.
BL654 PA series allows developers access to all of the nRF52840 hardware features and capabilities including USB access and up to 5.5V supply. It also adds additional TX power capabilities via an integrated Skyworks PA. In addition to Bluetooth 5's enhanced data rates and LE long-range, the BL654 PA also features BLE mesh capabilities in a high TX power platform, NFC, and Thread (802.15.4).
The BL654 PA also has robust security, industrial temperature rating, a small footprint, and modular FCC, IC, KC, RCM, and Bluetooth SIG approvals. Multiple low-cost development kits will also be available.

Laird Connectivity
www.lairdconnect.com/BL654-PA

Nordic and Quuppa enhance Bluetooth location services

Nordic Semiconductor and Quuppa will work together to allow Quuppa's Intelligent Locating System to operate on Nordic's nRF52 Series SoCs.
The two companies have been partners since 2016 and the latest firmware running on Nordic's nRF52832 BLE/Bluetooth 5 SoC, uses the Bluetooth LE protocol to transmit the 'Angle-of-Arrival' (AoA) radio packets which determine the position in space of a Bluetooth LE transceiver. Bluetooth 5.1 Direction Finding improves on this technique by providing simplified access to the Bluetooth LE protocol's IQ signal data for the Quuppa positioning engine. The technology has been employed by major Bluetooth beacon and tag manufacturers for tracking applications with accuracies down to a few centimetres.
Quuppa's previous long-term experience working with Nordic's nRF52 Series architecture will significantly extend the ecosystem of RTLS solution providers and applications based on the technology. Further expansion will be encouraged by Bluetooth 5.1 Direction Finding's interoperability between products from different vendors and the next generation of smartphones.
Nordic's nRF52811 SoC is one of the first Bluetooth 5.1-compatible commercial solutions and incorporates a 64MHz, 32-bit Arm Cortex M4 processor which provides ample overhead for supervising both the Bluetooth RF software protocol and the RF profile positioning engine firmware.

Nordic Semiconductor
www.nordicsemi.com

Making the Right Choice: Wireless Technologies for the IoT

By Anders Pettersson, Silicon Labs

Wireless connectivity is a critical part of IoT end-node design. Important and popular connectivity options for the IoT include Bluetooth Low Energy (LE), Bluetooth mesh, Zigbee, Thread, Z-Wave, Wi-Fi and a wide range of proprietary protocols in the sub-GHz band.

There are many use cases for IoT devices, requiring a range of connectivity capabilities. For example, Wi-Fi is often used in Internet protocol (IP) cameras and devices with streaming content. Bluetooth is ideal for commissioning a variety of smart home devices and other applications. Zigbee, Thread, Z-Wave and Bluetooth mesh support large networks of interoperable devices, such as smart lighting, energy monitoring and home security systems.

Figure 1: Bluetooth mesh enables many-to-many device communications for IoT environments such as the smart home.

Each wireless protocol offers its own blend of features and characteristics, and picking the right one depends on the end product's requirements. Think about how it will be used and how it fits in a wider ecosystem. This will guide your decision and help you address considerations around energy efficiency, performance, security, interoperability, upgradability and interference with other RF sources.

Let's look at each of these popular connectivity options in turn.

Bluetooth

Bluetooth is a popular and ubiquitous protocol that has evolved over time. Its first official specification was released in 1999 by the Bluetooth SIG. What started as a protocol for mobile headsets and streaming voice/audio data has evolved into a powerful and yet energy-efficient wireless technology, with Bluetooth Low Energy (LE) now being most popular for power-sensitive IoT end-node applications.

The Bluetooth LE specification supports very-low-power operation. To work reliably in the 2.4 GHz frequency band, it leverages a robust frequency-hopping spread spectrum approach that transmits data over 40 channels. With the enhancements in Bluetooth v5.0, Bluetooth LE offers a tremendous amount of flexibility for IoT designs, including multiple physical layer (PHY) options that support data rates from 125 kbps to 2 Mbps, multiple power levels (from 1 mW to 100 mW), and multiple security options, up to government grade.

The launch of Bluetooth mesh in mid-2017 added yet another mesh networking option for the IoT. Bluetooth mesh networking enables many-to-many device communications and is well-suited to creating IoT solutions where tens, hundreds or even thousands of devices must reliably and securely communicate with each other. Bluetooth mesh devices are ideal for smart home, lighting, beaconing and asset-tracking applications. In retail marketing and asset-tracking, for example, Bluetooth mesh technology simplifies the deployment and management of beacons. By combining Bluetooth LE with mesh networking, new capabilities and value can be introduced into IoT devices, such as connected lights that also serve as beacons or beacon scanners.

Zigbee

First standardized in 2004 by the Zigbee Alliance, Zigbee operates on the IEEE 802.15.4 physical radio specification and features lower power consumption relative to Bluetooth and Wi-Fi. Due to its mesh topology and proven scalability to easily support networks with over 250 nodes, it's widely used in home automation and industrial mesh networks.

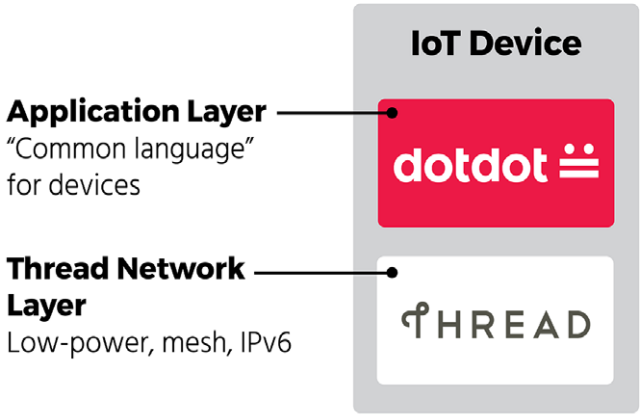


Figure 2: Dotdot provides a common application layer for the IoT.

The combination of low-power capability and 'self-healing' scalability makes Zigbee unique. Adopting the 802.15.4 MAC/PHY with short packet sizes, the 16-channel direct-sequence spread spectrum (DSSS) modulation scheme, and MAC-layer mechanisms for message-failure handling, Zigbee can operate within low-power envelopes. Moreover, the output transmitter power can be configured to conserve power, especially in

concentrated networks where battery-powered 'routing nodes' are nearby to help relay messages. This optimized method for handling mesh routing functions keeps memory resource needs relatively low, with less than 160 kB flash and typically 32 kB of RAM needed. This enables lower-cost silicon and ultimately more-economical solutions for application developers and consumers.

The Zigbee Alliance has also specified application profiles, known as cluster libraries, to simplify the development of standard products such as light bulbs and occupancy sensors. The common Zigbee application layer for the IoT is known as Dotdot, a universal, standard application language for smart devices to communicate over any network, such as Thread.

Thread

Thread is the most recent wireless technology to emerge for the IoT, providing IP-based mesh networking and advanced security. The Thread Group, founded in 2014, released the Thread specification in July 2015 and has continued to enhance it. Thread is based on a foundation of existing standards, including IEEE 802.15.4, and adds special design specifications for the network and transport layers. Like Zigbee, Thread operates in the 2.4 GHz frequency band and forms a robust, self-healing mesh network of up to 250 nodes.

Thread supports low-power, low-cost, mesh scalability, security and native IP addressing. Similar to Zigbee, it offloads some of the complexity of mesh neighbor processing to static memory 'lookup tables', while also keeping the transport/routing resource needs relatively low to operate on low-cost embedded devices (with less than 185 kB flash and 32 kB of RAM needed).

Accomplishing this is largely a software effort, which is why Thread solutions and stack providers take pride in developing and offering robust solutions to implement on the host silicon, typically a wireless microcontroller (MCU) or system-on-chip (SoC) device. As flash memory has become cheaper and integrated circuits (ICs) have incorporated more memory, the low/medium memory requirements of Thread stacks have enabled chip integration of more RF components, such as inductive matching networks. This frees developers from the complexities of RF engineering.

Z-Wave

Z-Wave technology is an open, internationally recognized International Telecommunication Union (ITU) standard (G.9959). It's one of the leading wireless smart home technologies available today, with more than 2,400 certified interoperable products worldwide. Represented by the Z-Wave Alliance and supported by more than 700 companies around the world, Z-Wave is a key enabler of smart living solutions for home safety and security, energy, hospitality, office and light commercial applications. Z-Wave technology was developed in 1999 by Zensys, a Copenhagen-based start-up, later acquired by Sigma Designs in December 2008, and most recently acquired by Silicon Labs in April 2018.

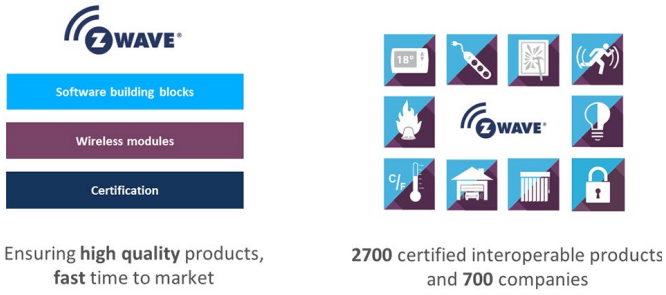


Figure 3: Z-Wave is used by more than 700 companies in more than 2,700 certified interoperable products worldwide.

One key attraction of Z-Wave is that it provides mesh networking on sub-GHz frequency bands, avoiding the sometimes crowded 2.4 GHz industrial, scientific and medical (ISM) band, which most of the other standards-based IoT protocols use.

Interoperability and backward-compatibility are key tenets of Z-Wave's technology philosophy. This outlook has garnered many fans in the device-manufacturing and ecosystem space,

Intel launches new high-performance FPGA acceleration card

Intel's new FPGA Programmable Acceleration Card D5005 will provide more acceleration capacity for Hewlett Packard Enterprise's (HPE) ProLiant DL380 Gen10 server.

The new accelerator is intended to target computing-intensive markets, such as streaming analytics, media transcoding, and network security. The high-performance Intel FPGA Programmable Acceleration Card (Intel FPGA PAC) D5005 offers more logic, memory and networking capability than previous PACs. It has been qualified in the HPE ProLiant DL380 Gen10 server, providing a higher performance option than Intel's earlier PAC built on the Intel Arria 10 GX FPGA.

Intel FPGA PAC D5005 acceleration card is based on an Intel Stratix 10 SX FPGA. It provides high-performance inline and lookaside workload acceleration to servers based on Intel Xeon Scalable processors using the Intel Acceleration Stack.

HPE is the first server OEM to announce pre-qualification of the Intel FPGA PAC D5005 accelerator card. Other server vendors are currently qualifying the PAC D5005.

Initial workloads specifically developed for the Intel FPGA PAC D5005 accelerator card include:

- AI (speech-to-text translation) from Myrtle*
- Network security from Algo-Logic*
- Image transcoding from CTAccel*
- Video transcoding from IBEX*

Compared to the Intel PAC with Intel Arria 10 GX FPGA, Intel FPGA PAC D5005 features more resources, including triple the amount of programmable logic, up to 32 GB of DDR4 memory (4x increase) and faster Ethernet ports (two 100GE ports versus one 40GE port). With a smaller physical and power footprint, the Intel PAC with Intel Arria 10 GX FPGA is intended for a broader range of servers.

Intel

https://buy.hpe.com/b2c/us/en/options/accelerators/computational-graphics-accelerators-for-servers/computational-graphics-accelerators-for-proliant-servers/intel-accelerators/p/1010912907

and serves as the backbone of the Z-Wave Alliance's success. The Alliance focuses on certifying Z-Wave product interoperability and on expanding marketing opportunities for members.

Wi-Fi 802.11b/g/n

Wi-Fi is built on the IEEE 802.11 specification for local area networks. It primarily addresses the need for higher-bandwidth IP networks in homes and businesses. Like many wireless IoT technologies, Wi-Fi operates in the 2.4 GHz frequency band. It also recently extended support to the 5 GHz band to address the challenges of achieving higher data rates and avoiding interference from other licensed 2.4 GHz technologies.

Figure 4: Multiprotocol connectivity opens up new use capabilities and use cases for the IoT.

Major Wi-Fi considerations include IP networking, bandwidth and power. Because they're typically geared for high bandwidth, high power usage and complex supporting software, Wi-Fi-based designs tend to be more expensive than other IoT technologies. Wi-Fi requires larger, more sophisticated RF components and more embedded computing resources for network processing. However, you get what you pay for, which is why Wi-Fi is the dominant player when you need data rates beyond 10 Mbps and direct access to the internet.

Looking ahead, we can expect Wi-Fi to continue to evolve with the IoT, which will likely mean lower power-consumption, faster speeds and combined hardware/software solutions for coexistence in the 2.4 GHz band (with Bluetooth and 802.15.4) and the 5 GHz band (with cellular).

Proprietary Sub-GHz

For low-data-rate applications such as industrial sensing, sub-GHz networks operating at frequencies below 1 GHz offer some benefits over more-powerful, feature-rich 2.4 GHz protocols. Range is the primary area where sub-GHz networks shine. Narrowband transmissions can operate uninterrupted for a kilometer or more, transmitting data to distant hubs without the need for more complex mesh software implementations to hop from node to node. The sub-GHz band is also less crowded than ISM 2.4 GHz.

That said, in some regions there are limited sub-GHz channels available, which prevents developers from producing a single-architecture global solution. A related drawback is that sub-GHz airwave regulations differ by country, and duty cycle restrictions may actually limit the application's transmission time.

Overall, sub-GHz networks win when it comes to range, but lack the standardization of the 2.4 GHz protocols we previously mentioned.

Multiprotocol Connectivity

As a result of combined hardware and software engineering efforts throughout the industry, we've seen a rapid rise of wireless MCUs and SoCs capable of supporting multiple wireless protocols. These multiprotocol devices open up new IoT capabilities, such as simplified device commissioning and Bluetooth beaconing while on other networks.

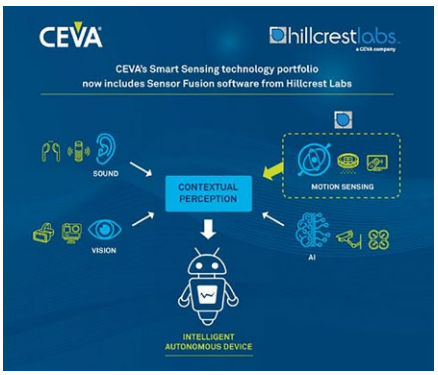
Multiprotocol SoCs also enable over-the-air (OTA) updates to deployed devices, drawing on the convenience of smartphones or tablets, and provide a simple means to add newer protocols such as Bluetooth LE to products with legacy proprietary protocols.

Advanced multiprotocol, multi-band SoCs from a number of suppliers are now providing greater flexibility and design options for developers seeking to add wireless connectivity, while simplifying their end-node designs.

https://www.silabs.com

CEVA acquires Hillcrest Labs intelligent sensor technologies

CEVA has acquired Hillcrest Laboratories, Inc. (Hillcrest Labs) business from InterDigital, Inc. Hillcrest Labs supplies software and components for sensor processing. Hillcrest Labs has over 15 years' experience in sensor processing and has shipped more than 100 million devices. The company is a leading innovator in data fusion from multiple sensors in intelligent systems. The resulting algorithms and software enable sensors and end user products to provide contextual awareness and a better user experience. Hillcrest Labs' MotionEngine software supports a broad range sensors and is licensed to companies that wish to run the software on CEVA DSPs, or a variety of RISC CPUs, including Arm Cortex-M and A series and RISC-V based cores.



MotionEngine software will expand and complement CEVA's smart sensing technology, which includes computer vision and AI processing for cameras and sound processing for microphones. CEVA DSP licensees will now be able use CEVA as a one-stop-shop for processing all classes and types of sensors. The Hillcrest Labs software technology will also widen CEVA's software licensing engagements directly with OEMs and ODMs to them to employ a royalty payment scheme based on devices rather than chips.

Further details of the transaction and related financial information will be disclosed in CEVA's Q2 2019 earnings conference call on August 8, 2019.

CEVA

www.ceva-dsp.com/app/motion-sensing/

Coding for IoT — Securing Software at Scale

Chuck Gehman, Perforce Software

Making sure that safety-critical connected products (such as driverless cars and medical devices) are secure and compliant is obvious. That's why there's been growing focus on software development processes over the past few years. Teams need to ensure that the processes involved in the creation of safety-critical connected products are safe, secure, and reliable. This has led to greater regulation and the use of coding standards.

Attention is turning to the development of more general consumer IoT devices and the challenges that are presented to the teams behind the creation of these software-dependent products. European CE and US LU certification applies to connected devices — not just those that are standalone.

Today, the scale of the IoT market, the pace at which software has to be developed, and the complexity that is often involved has created a tough IoT design environment. The development process is where the majority of software defects and vulnerabilities are introduced. Those vulnerabilities could potentially cause performance issues, product failure, or even be maliciously exploited at a later date.

Security is a growing concern — particularly since the Mirai botnet attack. The attack involved hackers taking over a large number of IoT devices and routers by using the passwords that were hard-coded in the factory. In addition, it was recently discovered by a 'whitehat hacker' that a popular lightbulb could be easily hacked to gain access to the Wi-Fi password for the user's home.

What a hacker or criminal could do with that kind of information ranges from the lightbulb example — which could enable them to unlock the doors of a house or turn off the security system — to crippling denial-of-service (DoS) attacks, such as the Mirai incident.

In the Mirai incident, hackers used IoT devices to launch distributed denial of service attacks (DDoS) and disrupted internet access for millions of companies and people globally. Modern consumer electronics are smart: plug them in and they will automatically find the Wi-Fi and connect to it, which is great functionality for the consumer, but also very useful for someone with malicious intent.

Programming Languages

The user interfaces for IoT tasks (such as remotely turning on lights or surveillance cameras) are typically developed using programming languages that have become popular for internet apps, including Node.js, Java, Python, and Go. Even though those programming languages are all relatively simple, they are secure. However, when it comes to the code in the actual IoT device, the most commonly used programming languages are Python and C.

The benefit of C is that it gives the developer far more control over the hardware along with far greater performance, flexibility, and scope for innovation. As a side note, the Linux operating system is written in C, which is why it is so much faster than Windows on comparable hardware.

However, unless a developer is familiar with it, C is very hard to understand. What's more, C relies on developers to make the right decision and not inadvertently introduce errors, such as accidentally over-writing memory. Unfortunately, human error is a common hazard in coding.

Market Pressures

While teams tasked with developing IoT devices are aware of the potential security risks, they are also under pressure to get products out to market fast. As so often happens in software development, corners may be cut. A common solution is to add more people to a project. While that may sound like an effective way to meet a deadline, it can also introduce new problems, such as relying on people who are less experienced, and placing more stress and responsibility on senior developers.

Of course, this is not always the case, and within organisations like Google and Amazon, there are highly efficient, well-defined software development processes. However, not every organisation has those kinds of resources. Plus, more traditional hardware-based companies moving to IoT development also have to adapt to accommodate a far more software-centric world. Generally kept separate, hardware and software teams now need to collaborate far more closely on the same projects,

often using many different systems, tools, and types of digital assets.

Critical Mass

With many different versions of a device in use, including legacy products that will need to be supported for their entire lifetime, software updates are frequent. This has led to the sheer speed and volume of software-based product development to reach an unprecedented scale.

As IoT moves toward the mass-market, we will see companies striving to introduce cheaper products, which means products with less memory and processing. To still give people the performance they want, companies will need to optimise software without overlooking security. There is a chance in

those situations that software development will become slower, more expensive, and riskier.

As IoT has become more mainstream, there has been an increase of expert 'bad guys' ready to exploit vulnerabilities. This is why many organisations involved in IoT are reviewing their development processes, team culture, methodologies, processes, and tools to ensure that they are efficient, effective, and secure.

Best Practices

For many of these organisations, the starting point is achieving better insight into the software development process. Knowledge of what is working — or what is not — makes it easier to prioritise what needs to be fixed.

For instance, coding standards — already common in safety-critical and compliance driven industries — are being more widely adopted. The idea is simple: Coding standards are sets of rules or guidelines for software engineering teams to observe. This gives them the confidence that the code they are creating is safe and compliant. To avoid creating additional workload for developers, coding standards are usually applied using static analysis tools.

Static analysis tools have long been used by traditional software development teams to continually inspect code for errors. Teams can use the tool right from the very start of a development project. The benefit of this practice is that the earlier a problem is discovered, the easier (and less expensive) it is to fix. What's more, static analysis can be deployed both inside and outside the Integrated Development Environment (IDE), so that code is inspected across both the build and execution stages.

Keeping It Continuous

Another big trend in software development is continuous testing. Testing has evolved from a routine 'tick-in-the-box' exercise to being at the heart of good software development. By testing early, often, and throughout the development process, developers can receive faster feedback. Also, the business can better identify quality-associated risks, such as bug fixes or new features.

Continuous testing fits in well with another popular concept, Shift Left. The concept involves developers taking on more responsibility for testing before it goes to QA managers or test engineers.

However, it is important not to confuse continuous testing with high-testing coverage, which lets developers know how much of their code is covered by automated tests. Using test automation tools helps to identify and execute the most relevant tests. While most organisations that use continuous testing are not 100 per cent automated yet, the percentage is increasing. What's more, the introduction of codeless testing and AI-based testing means that the skillsets are within reach of a far greater audience. No longer do individuals or teams have to become testing experts.

Visibility, Transparency, and Traceability

Development teams always need to be able to see the status of every contributor and change across a project, both in real-time and historically. This practice is often referred to as a 'single source of truth.' The idea is that at any time, it is possible to see who did what, when, where, and how. It is useful for organisations that need to be compliant as well as in regulation-light markets, such as games development.

This is because when a problem becomes apparent (like a bug), it is possible to not only pinpoint when and how it originated, but to also roll back to an earlier version of the software. A version control system can also show the interdependencies with other assets that are not code based, such as build artifacts, configuration data, and even graphics, sound, and movies.

Culture

Software development approaches need to complement the wider set of security tools and services, such as penetration testing. Development teams also need to consider code quality and security at each stage of development. These days, there is too much at stake to risk compromised code. Fortunately, there are a growing number of ways to address the challenges involved with managing code in the IoT era.

www.perforce.com

Nordic's Thingy:91 simplifies cellular IoT prototypes

Nordic Semiconductor's 'Thingy:91' rapid cellular IoT prototyping platform provides easy connectivity and integrated security.

Thingy:91 is certified for global, low-power, long-range LTE-M/NB-IoT applications. The device also features Arm TrustZone security, has a range of sensors, and provides embedded support with a Nordic nRF52840 advanced multiprotocol SoC for short-range wireless technologies such as Bluetooth 5, Thread, Zigbee, and ANT.

The devices also includes a Nano (4FF) eSIM card from iBasis with 10MB of data for out-of-the-box cellular LTE-M and NB-IoT connectivity.

The Nordic Thingy:91 is provided in a 6 x 6-cm plastic and rubber case with a USB connector fpr charging the internal 1440 mAh Li-ion battery. Environmental sensors include temperature, humidity, air quality, and air pressure, and colour and light. There are also separate low-power and high G-force accelerometers.

The nRF9160 is a low power SiP measuring 10 x 16 x 1mm, while integrating a dedicated application processor and a multimode LTE-M/NB-IoT modem. The application processor includes a 64MHz Arm Cortex-M33 CPU with 1MB Flash and 256KB RAM dedicated for the application. The nRF9160 SiP features ARM TrustZone and ARM CryptoCell, as well as a range of interfaces to communicate with sensors and actuators.

The nRF9160 SiP integrates GPS support to allow a combination of GPS and cellular data to be used for more accurate positioning.

The Nordic Thingy:91 can be programmed using Nordic's dedicated cellular IoT 'nRF Connect SDK' with integrated Zephyr RTOS.

Nordic Semiconductor'

www.nordicsemi.com/Products/Low-power-cellular-IoT/nRF9160

Farnell adds Kitronik products for micro:bit, Arduino and Raspberry Pi

Farnell has now added Kitronik products and accessories for micro:bit, Arduino and Raspberry Pi.

Kitronik kits and accessories are intended to foster interaction between programming and hardware. The products can support STEM education allowing beginners to learn electronics, coding and design.

Kitronik products and accessories for the micro:bit in stock at Farnell include:

• The Inventors Kit introduces programming and hardware interaction. It has everything needed for ten micro:bit experiments using LEDs, motors, light sensors and capacitors. The kit features a tutorial book. Circuits can be completed in minutes.

• The MOVE mini buggy kit allows a two-wheeled robot to be built that can be used for autonomous operation. It can also be controlled using Bluetooth or a second micro:bit. Five RGB Zip LEDs are individually addressable and can be used as indicators. Kitronik's custom code blocks for the Servo:Lite motors help make things easier to get going.

• The Kitronik: GAME ZIP 64 is a BBC micro:bit retro gaming accessory. It includes a built-in, 64 (8x8) individually addressable full colour Zip LED screen. It has on-board sound, four directional buttons, two fire buttons, haptic feedback, and breakout points. These features are fully programmable and breakout points allow for the use of larger LED screens.

Support for young engineers from Farnell includes free resources, including lesson plans, and project ideas from the Farnell website.

Farnell

www.farnell.com

Teltonika IoT Solutions in EMEA | Arrow

Arrow Electronics announced a distribution agreement with Teltonika, a Lithuania-based IoT solutions provider, covering Europe, Middle East and Africa (EMEA)

Teltonika offers a broad range of IoT-related solutions and has more than 100 different products in place. To date, it has sold more than 8.6 million devices worldwide. The company`s portfolio covers vehicle-tracking hardware and software on 2G, 3G, LTE, Bluetooth, GNSS, GPRS, NB-IoT and other connectivity options. The products feature a wide range of functionalities, including geofencing, over-the-air firmware updates, ignition detection, immobilizer, voice calls and many others. Teltonika also offers networking solutions including routers, gateways, modems and antennas for the enterprise network, as well as industrial M2M/IoT use. In addition, portable trackers are available for tracking cargo and other portable objects.

"Teltonika provides its customers with easy access to the world of IoT," says Paul Karrer, director of IoT for Arrow`s enterprise computing solutions business in EMEA. "A well-established provider, Teltonika has been equipping renowned enterprises and organizations across the globe with a multitude of products to enable smart communications and connectivity in many industry areas. Teltonika`s great variety of solutions, along with their IoT-focused networking products enable our channel customers to choose from an extensive selection to meet their end customers' individual IoT device and application requirements."

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